

Current Status and Advances in Damascene Electrodeposition

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Glossary

Additives Organic species intentionally added to a plating electrolyte.

Bottom-up filling or super-filling Process in which deposition occurs preferentially at the bottom of a feature rather than at the top.

CVD Chemical vapor deposition.

Interconnect Wire used to carry current in a semiconductor device.

PVD Physical vapor deposition.

TEM Transmission electron microscopy.

Trenches Features or cavities that have a rectangular cross-section.

Vias Cylindrical features or cavities that connect metal layers.

Wafer Thin slice of crystalline Si on which integrated circuits are made.

Nomenclature

D Mean grain width

i Plating rate (typically expressed as current density)

p Interface scattering factor

r Grain boundary reflection coefficient

R Resistance

x Film thickness

λ Electron mean free path

ρ Resistivity

Introduction

Integrated circuits, used in advanced electronics devices, enable applications such as high-speed computing and data storage. Nanoscale transistors and interconnects (represented schematically in Fig. 1A) form the two essential building blocks of an integrated circuit. The transistors perform the logic functions and the copper (Cu) interconnects provide the wiring between transistors. Modern electronics circuits routinely contain in excess of a billion transistors and interconnects. A two-dimensional cross-section image (acquired using a scanning electron microscope) of the interconnect network is shown in Fig. 1B. The multilayered interconnect network may consist of 7–10 interconnect levels, where the lower level interconnects are about 20–30 nm in critical dimension.

The process sequence used by the semiconductor industry to fabricate Cu interconnects is called the “dual-damascene” process. In this process (Fig. 2), nanoscale features including vias and trenches are first etched in a dielectric layer (typically porous SiO₂) followed by deposition of a 2–3 nm thick diffusion barrier layer. Sputter-deposited tantalum nitride (TaN) is conventionally used as a Cu diffusion barrier. A thin Cu seed layer is then sputtered, followed by bottom-up Cu electroplating to achieve void-free metallization of complex nanopatterns. Finally, excess Cu plated in the field regions is polished away using chemical mechanical polishing (CMP). This sequence of patterning, metal filling, and CMP is repeated sequentially to assemble the multilayered interconnect structure shown in Fig. 1B.

Nearly two decades ago, the semiconductor industry replaced then-used Al with Cu for interconnect fabrication due to numerous advantages that Cu offers. First, Cu has lower bulk electrical resistivity ($\sim 1.7 \mu\Omega \text{ cm}$) than Al. Second, Cu and Cu-alloys exhibit superior resistance to a degradation mode known as electromigration. Third, the dual-damascene interconnect fabrication flow reduces processing complexity substantially by enabling via and trench metallization essentially in one step. All these advantages offered by Cu are critical to ensuring low-cost manufacturing, high-performance, and reliable operation of advanced integrated circuits.

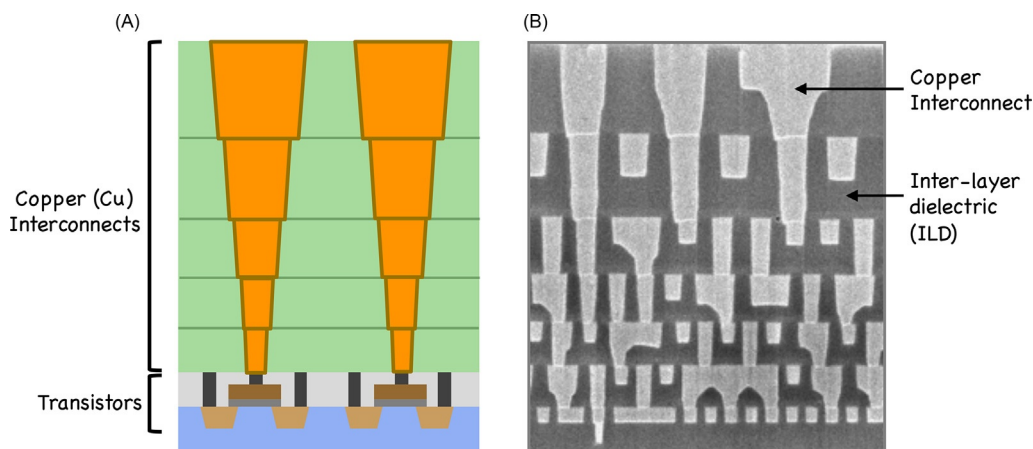


Fig. 1 (A) Schematic showing transistors and Cu interconnects which form the basic building blocks of an integrated circuit; and (B) a scanning electron microscope image showing the multilayered Cu interconnect structure. Fig. 1B is reprinted with permission from *Electrochimica Acta* 52, 2891 (2007). Copyright © 2006 Elsevier Ltd.

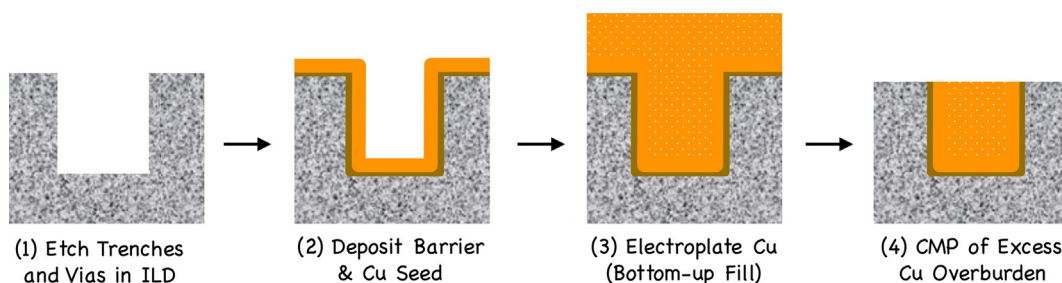


Fig. 2 Schematic of the interconnect fabrication flow consisting of patterning, metal deposition, and chemical mechanical polishing (CMP) process steps.

It is important to note that transistor and interconnect dimensions are continually shrinking in accordance with the Moore's law. The reduction in size allows increased number of device elements to be packaged onto a chip for increased performance. Future interconnect fabrication is likely to experience gradual evolution and at times disruptive revolution in the fabrication process sequence, the choice of the actual interconnect material used as well as architecture of the integrated device. This article presents first an overview of the state-of-the-art damascene Cu electroplating process, which enables metallization of semiconductor interconnects, and the fundamental electrochemistry underlying its operation. Future advances needed in electrochemical technologies to enable aggressive interconnect scaling are discussed in the second part of the article.

Electrolyte Additives Enable Bottom-Up Copper Electroplating

Early attempts to metalize patterned features, that is, vias and trenches, using Cu electroplating in the absence of electrolyte additives led to entrapment of voids and thus were deemed unsuccessful. In 1998, researchers at IBM demonstrated that electrolyte additives can enable preferential Cu deposition at the bottom of the patterned features eventually leading to void-free metallization. Electrolyte additives, such as polyethylene glycol (PEG) and bis-(3-sulfopropyl) disulfide (SPS), when present in ppm levels in the plating electrolyte can produce the so-called "super-filling" or "bottom-up" filling effect. A trench feature metalized partially with electroplated Cu in the presence of electrolyte additives is shown in Fig. 3. The microscopy image clearly demonstrates preferential Cu plating at the trench bottom and relatively suppressed deposition outside the feature, that is, in the field regions. If plating is continued, it would eventually lead to void-free filling of the trench. This concept of additives-assisted bottom-up Cu filling is at the heart of semiconductor device metallization and is the technology that enables void-free and reliable manufacturing of complex interconnect circuitry in modern devices.

The additives, that is, PEG and SPS, are surface-active molecules and exhibit a tendency to adsorb on the Cu surface during Cu electroplating. As these species adsorb onto the surface, they modify the Cu deposition kinetics. A schematic illustration of the Cu deposition kinetics in the presence of PEG or SPS is shown via the polarization curves in Fig. 3. When PEG adsorbs onto the Cu surface, it suppresses the deposition kinetics and hence PEG is called a "suppressor" additive. On the contrary, SPS depolarizes the Cu deposition reaction, as shown in Fig. 3, and thus SPS is called an "accelerator" additive. If favorable conditions exist (as discussed later), SPS adsorbs near the feature bottom and accelerates Cu growth at the bottom. PEG adsorbs on the feature

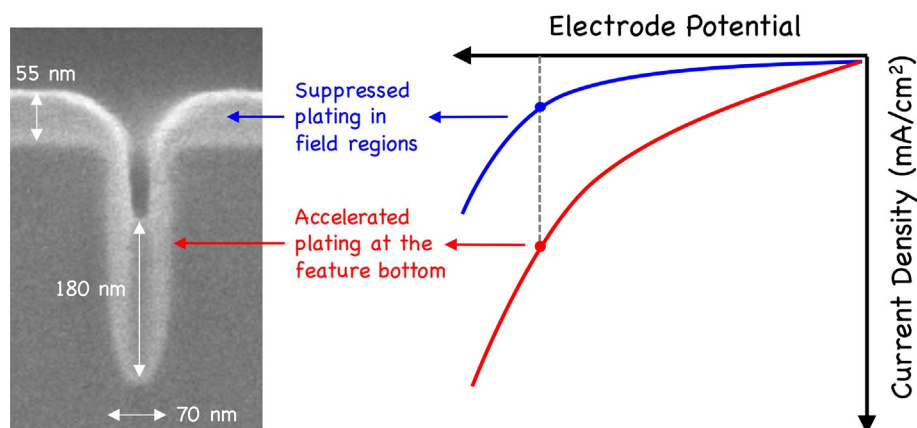


Fig. 3 Bottom-up filling of a trench is enabled using additives. A “suppressor” additive slows down deposition kinetics and operates in the field regions. An “accelerator” additive catalyzes deposition at the trench *bottom*. SEM image is reprinted with permission from *Electrochemical and Solid-State Letters*, 10 (6) D55 (2007). Copyright © 2007 The Electrochemical Society.

sidewalls and top surface and effectively suppresses Cu deposition in these regions. The combined effect of SPS and PEG adsorption at their respective locations produces a nonuniform growth profile, which leads to super-filling (or bottom-up filling) of the feature with electroplated Cu.

It is important to note that electrolyte additives, that is, PEG and SPS, interact on the surface during Cu electrodeposition. This is demonstrated in the schematic of an injection experiment in Fig. 4. During Cu electrodeposition onto a rotating disk electrode, the deposition current (under potentiostatic conditions) is altered by the sudden introduction (injection) of an additive in the plating electrolyte. When the suppressor PEG is introduced, the deposition current decreases gradually with time until a new steady-state current is reached. The new steady-state current represents a lower deposition rate as PEG adsorbs onto the Cu surface and blocks sites available for deposition. The rate-limiting step in the adsorption of PEG is its transport (diffusion) to the electrode surface, which may take 1–10 s depending on hydrodynamic conditions, the PEG concentration, and its molecular weight. As shown in Fig. 4, injecting SPS after the electrode is saturated with PEG leads to acceleration of the deposition kinetics (rate). After about 50–100 s, the PEG adsorbed on the electrode surface is completely displaced by SPS, suggesting that SPS adsorption is favored over PEG adsorption. If both SPS and PEG are injected at once, short time-scale PEG adsorption (suppression) followed by longer time-scale SPS adsorption (acceleration or antisuppression) is observed. Such experiments among others establish the intricate synergy between the additives used in damascene Cu electroplating.

Mechanisms for Bottom-Up Copper Electroplating

The mechanistic rationale behind additives-enabled bottom-up electroplating of Cu has been the subject of numerous studies over the last two decades. Models developed to explain how additives enable super-filling must provide a physicochemical basis to why acceleration is localized to the feature bottom surface. Early mechanisms proposed consisted of a single-component additive that diffuses slowly and is consumed during Cu plating. Since diffusion toward the feature bottom is even slower and the additive gets consumed during growth, its effective coverage at the feature bottom is low. This provides less blocking and thus faster Cu deposition kinetics, thereby initiating bottom-up plating. This one-additive model has some deficiencies. First, it does not explain why a two-component additive chemistry (consisting of PEG and SPS) is essential for super-filling. Second, it does not incorporate the additives interactions outlined in Fig. 4. Given these deficiencies, much effort was focused on developing improved process models and comparing the model predictions to experimental observations.

An important development in the understanding of Cu electrofilling was provided by the curvature enhanced accelerator coverage mechanism. This mechanism is based on changes in local surface area particularly at the feature bottom during super-filling (Fig. 5A). Near the feature bottom, conformal deposition during the initial stages leads to reduction in the local surface area available for additives adsorption. This causes enhancement in the local surface coverage of the strongly adsorbing accelerator SPS at the feature bottom as depicted in Fig. 5A. The enhanced catalyst, that is, SPS coverage then accelerates the Cu deposition kinetics and ensures a high Cu plating rate at the feature bottom. The continuation of the rapid Cu growth even after feature fill is completed results in “bump” formation—a phenomenon widely observed in semiconductor metallization.

Transient additives diffusion also plays an important role during bottom-up filling of high aspect ratio structures. The PEG, which is a large molecule and thus diffuses slowly, requires time to reach the feature bottom. The SPS, which diffuses relatively rapidly, reaches the feature bottom earlier than the PEG. SPS can thus rapidly adsorb on the feature bottom and reach a higher surface coverage than at the feature top surface. At the feature top, the PEG and SPS do not encounter substantial transport limitations. Under these conditions, the PEG adsorbs first and develops a higher coverage there. This intricate balance between

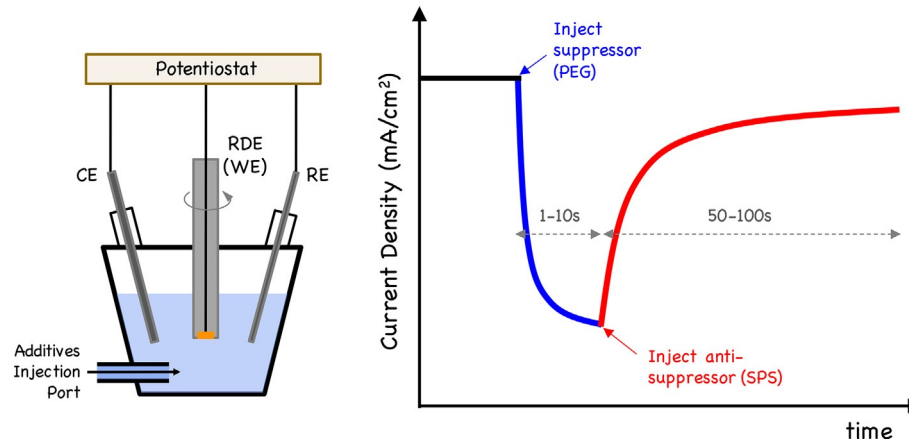


Fig. 4 Injection experiments to characterize the additives (PEG and SPS) function and the associated chronoamperometric response.

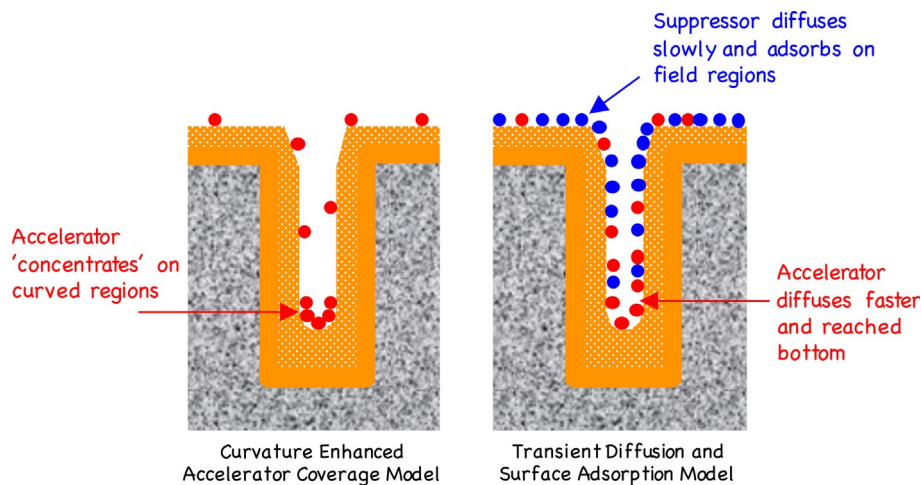


Fig. 5 Schematic representation of some of the mechanisms available in literature that describe how additives adsorption and interactions lead to super-filling.

diffusion and surface adsorption rates of PEG and SPS is the crucial driving force for bottom-up filling of very high aspect ratio structures.

In recent years, sophisticated simulations of the bottom-up filling process have been made available. These simulations incorporate all the relevant additives mechanistic, thereby allowing precise determination of the filling profiles and their dependencies on a wide range of process parameters. The comprehensive understanding of additives behavior in the context of damascene Cu electroplating has impacted many other technologically significant areas, including through-silicon-via metallization and even the fabrication of composite materials using electrodeposition into porous matrices. It has also triggered the development and understanding of additives chemistries for the electroplating of many other metals and alloys.

Practical Issues in Wafer Metallization by Cu Electroplating

Wafer-scale current distribution: During semiconductor processing, 300-mm diameter Si wafers are first patterned using lithography and the billions of interconnect features are then metalized with Cu metal all at once. Electrical contact must be made to the PVD Cu seed so that external current can be passed during the Cu electroplating step. Since contact is made at the periphery of the wafer and thin (~20 nm) Cu seed layers are electrically resistive, the applied current is utilized for the plating reaction preferentially at the wafer edge. This leads to nonuniform wafer-scale distribution of the plating rate. A simplified equivalent circuit diagram describing this effect is shown in Fig. 6. The ratio of the wafer center plating rate (i_{ctr}) to the wafer edge plating rate (i_{edge}) depends on the electrolyte resistance ($R_{electrolyte}$) and the seed resistance (R_{seed}) as:

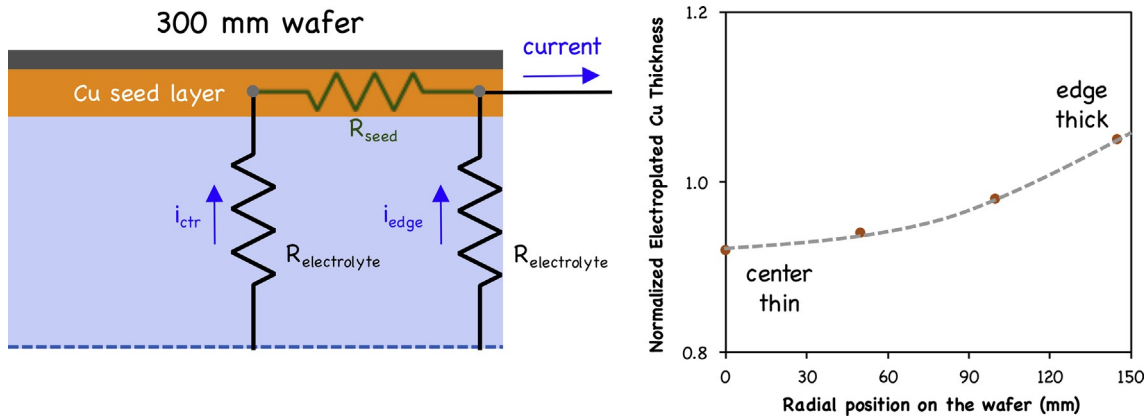


Fig. 6 An equivalent circuit diagram that explains the terminal effect during Cu plating on 300 mm wafers, which leads to nonuniform thickness distribution when using resistive seed layers.

$$\frac{i_{\text{ctr}}}{i_{\text{edge}}} = \frac{R_{\text{electrolyte}}}{R_{\text{electrolyte}} + R_{\text{seed}}}$$

For resistive seed layers (high R_{seed}), the ratio $i_{\text{ctr}}/i_{\text{edge}}$ is low and this explains the nonuniformity of the wafer-scale plating distribution as seen in the experimentally measured normalized Cu thickness profile on a 300-mm wafer (Fig. 6). To bring $i_{\text{ctr}}/i_{\text{edge}}$ close to 1, $R_{\text{electrolyte}}$ must be increased so that $R_{\text{electrolyte}} \gg R_{\text{seed}}$. This may be accomplished using low-acid plating electrolytes and resistive insulator elements in the electrolyte compartment of the plating cell.

Additives inclusion and its effect on Cu resistivity: The role of additives in enabling super-filling is important; however, the adsorbed additives may also get incorporated in the Cu deposit. The presence of sulfur, oxygen, and chlorine in the ppm range, confirmed via mass spectroscopy measurements, is due to additives incorporation. The incorporation of many impurity elements in the Cu deposit may retard the Cu grain growth and increase the electrical resistivity of the Cu plated inside the features. This is an undesirable effect as it increases the signal delay of the interconnect structure. Additives incorporation and their segregation at interfaces may also affect the electromigration resistance of the interconnects.

Wafer entry and feature fill times: As shown in the partial fill image in Fig. 7, the time required for feature fill depends on the feature size. For 45 nm features, fill times are typically in the 5–10 s range. However, as feature sizes approach 10 nm, feature filling is complete in just about 1 s or less. This presents significant challenges. First, the diffusion, adsorption, and surface interactions of the additives (PEG and SPS) must be tuned so that effective super-filling process takes place in the timescale of ~ 1 s. Second, optimizing the process of wafer entry into the plating electrolyte is crucial. Parameters such as entry angle, wafer rotation and entry speed, and the applied potential or current waveforms during entry must be optimized to ensure that the basic additives chemistry is unaffected particularly during the first few seconds after the substrate is introduced into the plating electrolyte. “Hot” entry of the wafer into the plating bath is essential to instantaneously initiate plating, thereby avoiding dissolution of the extremely thin Cu seed layers that coat the sidewalls of high aspect ratio structures particularly for advanced semiconductor technology nodes.

In addition to aforementioned issues, many other issues of practical relevance are intricately tied to the additives chemistry. These include “bump formation” during overburden plating and its control using levelers, the uneven plating at the die-level due to nonuniform additives transport, and the effect of additives incorporation on Cu electromigration resistance, to name a few.

Emerging Technologies for Future Damascene Plating Applications

For future nanoscale interconnects, improved additives chemistries are needed for achieving void-free super-filling of high aspect ratio structures. However, for sub-10 nm features, new additives chemistries by themselves are unlikely to address the challenges associated with metallization of such aggressive geometries. Beyond the 10 nm technology node, radical changes will likely be needed to the way in which feature metallization is carried out. In this section, some of the emerging and disruptive technologies that may provide solutions for future-generation metallization are reviewed.

Direct Cu electroplating on noble liners: The PVD Cu seed layers used in conventional dual-damascene metallization develop overhang, that is, excessive deposition of Cu during PVD at the feature opening. This leads to nonuniform seed coverage. The excessive overhang may lead to pinch-off prior to the Cu electroplating step. This issue poses severe limitations to the extendibility of PVD Cu seed layers in future metallization schemes. To circumvent this issue, noble metal liners, for example, ruthenium (Ru), are being considered. Ru is noble, electrically conductive, and does not corrode in acid Cu plating baths. CVD and atomic layer deposition (ALD) processes for fabricating highly conformal and thin (~ 2 nm) Ru liners on 300 mm wafers are commercially available. Utilization of Ru liners necessitates a complete re-engineering of the Cu electroplating process. First, when electroplating Cu on a Ru liner, electronucleation effects dominate and this leads to heterogeneous growth of Cu islands rather than uniform

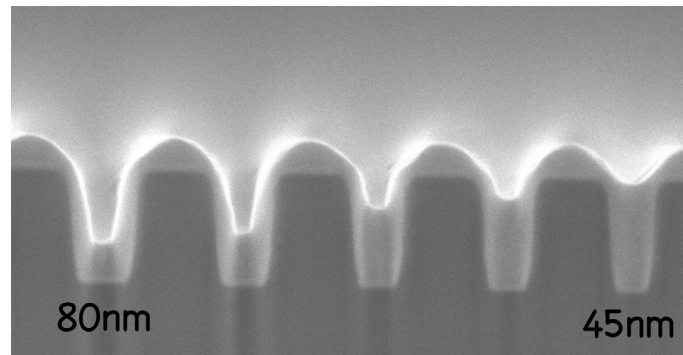


Fig. 7 The rate of bottom-up filling is strongly dependent on the size of the trench to be filled. Reprinted with permission from *Electrochemical and Solid-State Letters*, 10 (6) D55 (2007). Copyright © 2007 The Electrochemical Society.

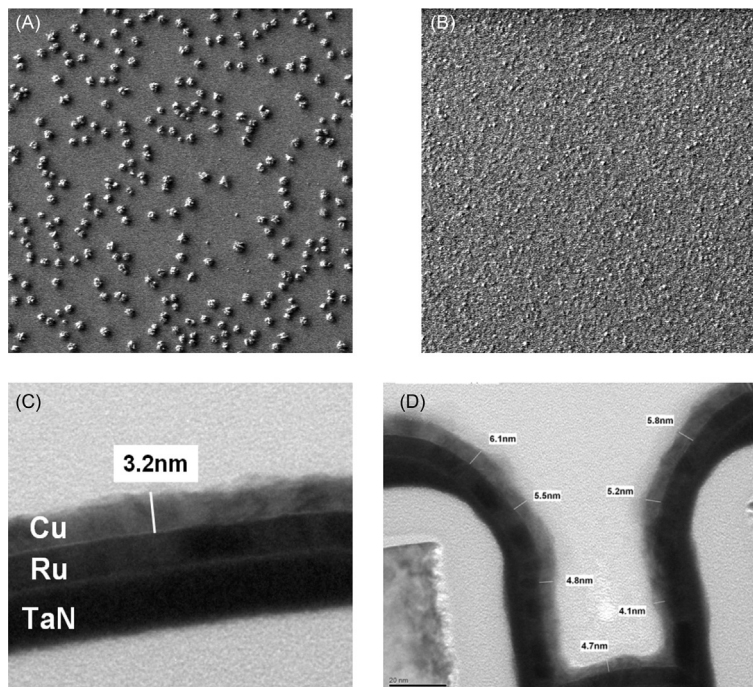


Fig. 8 (A) Cu nuclei formed on a Ru substrate during electroplating; (B) improved Cu nucleation [compared to (A)] leading to early film coalescence during plating; (C) nanofilms of Cu electrodeposited on Ru using a “wet” process; and (D) wet-seed enables uniform, conformal and smooth seed layers to be fabricated on patterned geometries. Reprinted with permission from *IEEE International Interconnect Technology* (2011). Copyright © 2011 IEEE.

deposition of a thin Cu film (Fig. 8A). As plating is continued, the Cu nuclei grow and eventually coalesce to form a film. To achieve early coalescence (needed for thin-film deposition, i.e., ~1 to 2 nm), the electroplating process must be modified. Use of nucleation promoting additives, current or potential pulsing, complexed electrolytes including those with alkaline pH, and pretreatments of the underlying Ru surface to remove surface oxides and other contaminants such as carbon (introduced during the CVD/ALD Ru growth process) have been studied. Fig. 8B and C shows top-down and cross-section TEM images of one such optimized Cu electroplating process called “wet-seed.” This process enables electrochemical fabrication of thin (~3 nm) Cu seed layers via direct plating onto Ru. The excellent conformality of the Cu wet-seed process on a patterned substrate is seen in the cross-section TEM image in Fig. 8D. At present, semiconductor technology does not use liners or direct plating; however, R&D in such technologies is ongoing at many major semiconductor equipment manufacturers.

Electroless deposition: As described earlier, one of the main technical challenges in wafer metallization by electroplating is the wafer-scale current (or deposit) distribution. In contrast to electroplating, electroless plating does not require an external applied current or potential. In electroless deposition, soluble reductants (e.g., aldehydes) are added to the plating electrolyte and these reductants enable deposition of the Cu metal onto a catalytically active substrate. Since the overall deposition reaction does not require current flow through a resistive seed layer, the uniformity of the deposit distribution is substantially improved. Thus, for future 450 mm wafer metallization, electroless deposition is a potential candidate. Achieving bottom-up filling in electroless

deposition has been a long-standing problem which has received much attention in recent years. Some additives chemistries that exhibit bottom-up filling in electroless Cu deposition have been proposed by Prof. Shingubara and his colleagues. A single-additive electroless chemistry containing SPS was shown to enable void-free filling in narrow trenches. Here, SPS serves to suppress electroless plating in the field regions unlike classical electroplating where SPS is an accelerator. Slow diffusion and incorporation of SPS inside the trench leads to low SPS coverage at the bottom and thus breakdown of suppression, leading to preferential plating in a bottom-up mode. In spite of such promising efforts, electroless super-filling of aggressive (sub-20 nm) structures is not adequately mature and the fundamental understanding of the additive chemistry requires more work. In the context of direct plating on noble metal liners, electroless plating is also a candidate because it offers improved nucleation density and enables the fabrication of thin and conformal seed layers.

Electrochemical atomic layer deposition (e-ALD): In fabricating future sub-5 nm interconnects, metal deposition will require unprecedented atomic-level control and precision not encountered thus far in classical damascene processing. Inspired by vapor-phase ALD, an electrochemical method for atomic layer-by-layer assembly of metals has been developed over the last two decades. This process is widely known as e-ALD. e-ALD has been used to fabricate nanolayers of Pt, Cu, Pd, Ru, and many other metals. A recently developed embodiment of e-ALD that is particularly suited for semiconductor applications is shown in Fig. 9. This process uses stable, nontoxic, water-soluble, and widely available salts as the deposition precursors. Electrode potential manipulation coupled with surface-limited reactions allows atomic layer-by-layer deposition with unprecedented control over thickness, roughness, composition, conformality, and wafer-scale uniformity. The Cu e-ALD sequence consists of two steps repeated sequentially: (i) underpotential deposition (UPD) of a sacrificial atomic layer of a suitable metal M (e.g., Zn) at an applied electrode potential E_{UPD} ; followed by (ii) releasing the electrode potential to trigger the spontaneous displacement of the sacrificial M-layer by a nobler Cu atomic layer. Repeated cycles enable growth of nearly atomically flat deposits with precise control. Implementation of e-ALD in a “one-pot” configuration and the use of optimized potential pulsing sequences have paved the way for high-throughput processing. Modern e-ALD chemistries do not use toxic chemicals (unlike conventional e-ALD chemistries) and this makes e-ALD attractive from a scalability and commercial viability perspective. Electrochemical ALD of other active metals (e.g., Co) has also been demonstrated. Preliminary mathematical models show that e-ALD can be readily implemented on 300-mm wafer-scale plating tools. The self-limited e-ALD growth mode circumvents the need for complex hardware designs to tackle terminal effects in traditional electroplating reactors.

Emerging interconnect materials: The Cu metal loses its conductive properties at narrow dimensions. Due to electron scattering in nanoscale metallic films, an inverse relationship between the electrical resistivity and film thickness is observed. The resistivity of nanofilms increases due to two effects: (i) increased scattering of electrons at interfaces in the film per the Fuchs–Sondheimer model and (ii) increased scattering of electrons at grain boundaries in the film in accordance with the Mayadas–Shatzkes model. The two effects can be incorporated into the following resistivity–thickness relationship:

$$\rho = \rho_b \left[1 + \frac{3}{8}(1-p)\frac{\lambda}{x} + \frac{3}{2}\left(\frac{r}{1-r}\right)\frac{\lambda}{D} \right]$$

where ρ_b is the bulk resistivity, x is the film thickness, λ is the electron mean free path, p is the interface scattering factor, r is the grain boundary reflection coefficient, and D is the mean grain width. Assuming that, for crystallized films, D approaches the film thickness, and using $r=0.5$, $p=0$, $\lambda=39$ nm, and $\rho_b=1.7$ $\mu\Omega$ cm, we get $\rho=14.1$ $\mu\Omega$ cm for a Cu film of $x=10$ nm thickness. This

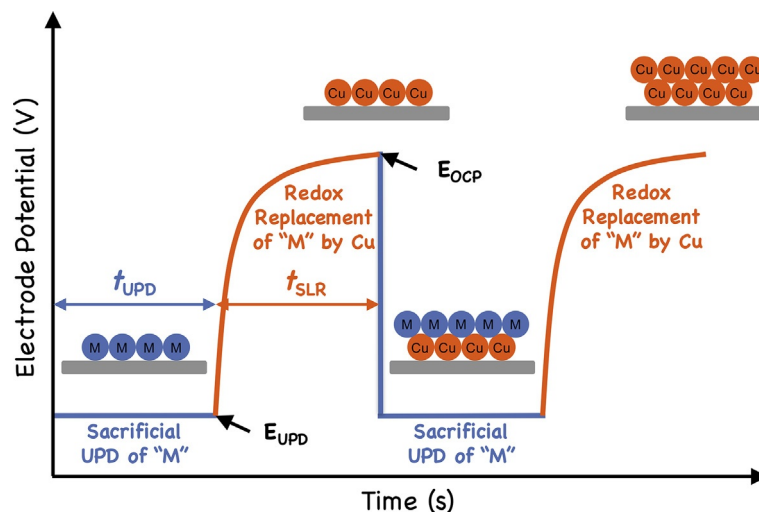


Fig. 9 Schematic of an electrochemical atomic layer deposition (e-ALD) sequence, which enables Cu deposition with atomic-level precision and control. In this process, a sacrificial atomic layer of metal M (e.g., M=Zn) is first underpotentially deposited (UPD). Then, the UPD layer undergoes spontaneous redox replacement (SLRR) by an atomic layer of Cu. Repeat UPD-SLRR cycles can be used to create multilayered films.

Table 1 Short list of potential candidate interconnect metals, their room temperature, bulk resistivity, and electron mean free path values

<i>Metal</i>	<i>Bulk resistivity ($\mu\Omega\text{ cm}$)</i>	<i>Electron mean free path (at room temperature) (nm)</i>
Cu	1.7	39
Al	2.6	19
W	5.3	16
Co	6.2	7–12
Ni	6.9	~6
Ru	7.8	4–7

(Source: D. Gall, *J. Appl. Phys.*, 119, 085101 (2016))

shows that nanofilms of Cu have substantially higher resistivity and may not be suitable for interconnect applications where the critical interconnect dimension is below 10 nm. Thus, alternative interconnect materials are being investigated which exhibit very low electron mean free paths (λ). If λ is low, the electron scattering components in the above resistivity–thickness relationship can be minimized. This may allow the use of interconnect materials such as Co ($\lambda = 7$ nm), which exhibit higher bulk resistivity than Cu but comparable thin-film resistivity at narrow ($x < 10$ nm) dimensions. Cobalt is also likely to provide improved electromigration resistance. Co electroplating chemistries and additives tailored to achieve Co super-filling are also being researched by many investigators around the world. A short list of candidate interconnect materials for future semiconductor applications and their electron mean free paths is provided in [Table 1](#).

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